REMARKS

Claims 1, and 27 - 135 remain in this application. No claims have been cancelled. Claims 128-135 have been added. Claims 33, 34, 37, 40, 44, 45, 91, 94, 116, 120, 121, and 122 have been amended. Replacement of "representing" with "including" and replacement of "paired" with "grouped" are broadening amendments. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §112 Rejection

The Examiner has rejected claims 33, 91-100, and 116-127 under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant claims as the invention.

Claim 33 has been amended to depend from claim 32 instead of claim 27. This amendment was to correct an error and is not a narrowing amendment.

Claims 91, 116, 120, 121, and 122 have each been amended to recite that M is "an even number". Applicants respectfully submit that these amendments are not narrowing amendments.

It is believed that these amendments properly address the rejection under 35 U.S.C. §112, second paragraph, and the Applicants respectfully request that the rejection be removed.

35 U.S.C. §101 Rejection

The Examiner has rejected claims 34-39 and 45-47 under 35 U.S.C. §101 because the claimed invention is allegedly directed to non-statutory subject matter.

Claim 34 has been amended to overcome the rejection under 35 U.S.C. §101 by limiting it to a processor-implemented method and by clarifying that the operations are performed responsive to the execution of the single instruction in that the third packed data is "for use as an operand to another instruction following the single instruction." Thus, the claim requires a processor that includes specific logic because it must be able to perform the claimed operations responsive to a single instruction.

Claim 37 has been amended to overcome the rejection under 35 U.S.C. §101 by clarifying that the method is a processor-implemented method and by clarifying that the operations are performed responsive to the execution of the single instruction. Thus, the claim requires a processor that includes specific logic because it must be able to perform the claimed operations responsive to a single instruction.

Claim 45 has been amended to overcome the rejection under 35 U.S.C. §101 by clarifying that the method is a processor-implemented method. The method is also performed responsive to execution of the single instruction. And the "adding" operations are performed in "parallel." Thus, the claim requires a processor that includes specific logic because it must be able to perform the claimed operations responsive to a single instruction.

It is believed that these amendments properly address the rejection of claims 34-39 and 45-47 under 35 U.S.C. §101, and the Applicants respectfully request that the rejection be removed.

Double Patenting

The Examiner has provisionally rejected claims 32-36, 37, and 40-47 under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 1-9 of U.S. Patent No. 6,385,634.

The Examiner has provisionally rejected claims 1, 32, 34, 37, 40, 45, 48, 62, 82, 91, 101, 116, and 120-122 under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over at least claims 1, 7, and 13 of U.S. Patent No. 5,859,997.

The Examiner has provisionally rejected claims 1, 32, 34, 37, 40, 45, 48, 62, 82, 91, 101, 116, and 120-122 under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over at least claims 1-2, 6, 11, 18, 20, 22, and 24 of U.S. Patent No 5,983,256.

Applicants submit herewith a Terminal Disclaimer in compliance with 37 C.F.R 1.321 in reference to U.S. Patent No. 6,385,634, U.S. Patent No. 5,859,997, and U.S. Patent No 5,983,256, to overcome the above-identified double patenting rejections. Additionally, for the record, the Applicants submit that the present claims and the claims of U.S. Patent No. 6,385,634, U.S. Patent No. 5,859,997, and U.S. Patent No 5,983,256 were commonly owned by, or subject to an obligation of assignment to, the same entity at the time the inventions were made.

It is believed that the Terminal Disclaimer properly addresses the above-identified double patenting rejections, and the Applicants respectfully request that the rejections be removed.

35 U.S.C. §102(b) Rejection – Guttag

The Examiner has rejected claims 1, 29 and 40-44 under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,370,558 issued to Guttag et al. (hereinafter referred to as "Guttag"). The Office Action states, at lines 6-7 on page 5,

"Guttag et al. teach, e.g., see Figs. 5 and 12, the claimed invention. Also, see claim 1[1]; col. 6, lines 19-27, col. 21, lines 24-34, and col. 35, line 8 to col. 36, line 32." [2] The Applicants respectfully submit that Guttag does not anticipate the present claims.

Claim 40 recites "*In a computer system having stored therein a first packed data and a second packed data each containing initial data elements, each of said initial data elements in said first packed data having a corresponding initial data element in said second packed data, a method for performing multiply add operations in response to a single instruction, said method comprising: multiplying together said corresponding initial data elements in said first packed data and said second packed data to generate corresponding intermediate data elements, said intermediate data elements being divided into a number of sets; generating a plurality of result data elements, a first of said plurality of result data elements including the sum of said intermediate result data elements in a first of said number of sets, a second of said plurality of result data elements including the sum of said intermediate result data elements in a second of said*

[1] In rejecting the claims, the Examiner has relied in part on claim 1 of Guttag. Applicants believe that claims 1-7 and 17-23 of Guttag are not prior art to the present patent application. Guttag is a divisional of U.S. Pat. No. 6,240,437 filed Nov. 11, 1997; which is a divisional of U.S. Pat. No. 5,742,438 filed Apr. 15, 1996; which is a divisional of U.S. Pat. No. 5,509,129 filed Nov. 30, 1993. Claims 1-7 and 17-23 were not part of the original disclosure of U.S. Pat. No. 5,509,129. Applicants have located the file wrapper of Guttag and have learned that the claims apparently correspond to the non-elected Group II claims from U.S. Patent Application Ser. No. 08/967,102. Applicants have requested the file wrapper of U.S. Patent Application Serial No. 08/967,102 from the U.S.P.T.O on February 8, 2006 but it has still not been provided at the time of filing this response. Accordingly, Applicants are unable to confirm when the claims 1-7 and 17-23 were first introduced. Applicants believe that claims 1-7 and 17-23 were first introduced after the August 31, 1995 priority date of the present patent application. If this is the case, then Applicants respectfully submit that claims 1-7 and 17-23 are not prior art to the present patent application, and Applicants respectfully request that the examination be limited to those portions of Guttag that were part of the original disclosure of U.S. Pat. No. 5,509,129. Alternatively, if the Examiner intends to base the rejection on claims 1-7 and 17-23 of Guttag, then Applicants respectfully request that the Examiner clearly show that claims 1-7 and 17-23 of Guttag were first introduced prior to the August 31, 1995 priority date of the present application.

[2] The present Office Action uses only two lines of text to describe how a reference with 54 drawing sheets and 176 columns of text anticipates claims 1, 29, and 40-44. If the Examiner intends to maintain the rejection on Guttag, then the Applicants respectfully request that the Examiner be clearer as to which particular parts of Guttag the Examiner is using to reject which particular elements of claims 1, 29, and 40-44.

number of sets; and completing execution of said single instruction without summing said plurality of result data elements".

Guttag does not teach or suggest these limitations. In particular, Guttag does not teach or suggest generating result data elements each including a **sum of intermediate data elements generated by multiplying** together corresponding initial data elements in a first packed data and a second packed in response to a single instruction.

Guttag discusses "*a long instruction word controlling plural independent processor operations*" (see e.g., the Title). FIG. 5 illustrates in block diagram form a data unit 110. The data unit 110 includes a multiplier 220 and an arithmetic logic unit 230.

The arithmetic logic unit 230 includes three input ports for performing three input arithmetic and logic operations (see e.g., column 39, lines 39-42). As discussed at column 44, lines 2-5, "*Arithmetic logic unit 230 includes three input busses: input A bus 241 supplies an input to an A-port; input B bus 242 supplies an input to a B-port; and input C bus 242 supplies an input to a C-port*". The A, B, and C-ports are shown in FIG. 5. The data provided to a port may be from one of the registers 200 shown in FIG. 5 (see e.g., column 39, lines 54-55).

Table 21 at column 50 lists operations performed by the ALU. For example, the operation A+B is listed for Hex 66, and the operation A-B is listed for Hex 99. The A and B refer to the A- and B-ports of ALU 230. The Hex 66 in Table 21 is selected for MPYx||ADD instructions. See e.g., column 52, line 66 through column 53, line 4. MPYx||ADD refers collectively to: 1) **parallel** signed multiply and add (MPYS||ADD); and 2) **parallel** unsigned multiply and add (MPYU||ADD). The Hex 99 in Table 21 is selected for MPYx||SUB. See e.g., column 53, lines 5-10. MPYx||SUB refers collectively to: 1) **parallel** signed multiply and subtract (MPYS||SUB); and 2) **parallel** unsigned multiply and subtract (MPYS||SUB). See e.g., column 53, lines 1-10. The

parallel sign (||) is used to indicate that the multiply and arithmetic operations are performed in **parallel**. See e.g., column 116, lines 29-31. As discussed at column 111, lines 11-14, "*The instruction word alternatives are summarized as follows. The operation of data unit 110 may be a single ALU operation, or a single multiply operation, or one of each can be performed in **parallel*** (emphasis added)." Since the multiply and the add are performed in parallel, the output of the multiply is not used as the input to the add responsive to a single instruction.

In contrast, claim 40 pertains to generating result data elements each including a **sum of intermediate data elements generated by multiplying** together corresponding initial data elements in a first packed data and a second packed in response to a single instruction.

FIG. 43 further supports that the arithmetic operations are not performed on results of the multiply operations. FIG. 43 illustrates the format of the instruction word for digital image graphics processors (see e.g., column 110, lines 57-58). As discussed at column 111, lines 11-14, "*The instruction word alternatives are summarized as follows. The operation of data unit 110 may be a single arithmetic unit operation or a single multiply operation, or one of each can be performed in **parallel** (emphasis added)*".

Data unit formats A, B, C, D, and E are shown at the extreme right-hand side of FIG. 43. As discussed at column 116, lines 27-31, "*Data unit format E is recognized by bits 63-61 being "011". Data unit format E specifies **parallel** (emphasis added) arithmetic logic unit and multiply operations. These operations are referred to as "six operand operations" because of the six operands specified in this format. In the preferred embodiment the "operation" field (bits 60-57) specifies the operations shown below in Table 43. The symbol "||" indicates that the listed operations occur in **parallel** (emphasis added) within data unit 110.*" Applicants point out that MPYS||ADD,

MPYU||ADD, MPYS||SUB, and MPYS||SUB are clearly shown in Table 43 and are therefore six operand operations. The six operand instructions have four sources and two destinations (see e.g., column 117, lines 26-27. Notice in FIG. 43 for data format E that there are "src3", "dst2", "dst1", "src1", "src4", and "src2" fields (i.e., four sources and two destinations).

As discussed at column 118, lines 18-25 "*the first input to multiplier 220 on bus 201 is the register designated by the "src3" field (bits 56-54), the second input to multiplier 220 on bus 202 is the register designated by the "src4" field (bits 44-42), the input to barrel rotator 235 is the register designated by the "src1" field (bits 41-39) and the input to input A bus 241 is the register designated by the "src2" field (bits 47-45)*". FIG. 5 shows that the barrel rotator 235 is coupled to the B-port of the arithmetic logic unit 230 by the input B bus 242. As discussed at column 117, lines 33-34, "*If the instruction specifies a multiply operation, then "dst2"is the destination for multiplier 220*". As discussed at column 117, lines 36-38, "*The "dst1" field (bits 50-48) designates one of the data registers 200 as the destination for arithmetic logic unit 230*".

Notice that the "dst2" destination for the multiplier 220 is not used as an input source for the arithmetic logic unit 230. Instead, the "src1" and "src2" fields are used as input source for the arithmetic logic unit 230. The result generated by the multiplier 220 is sent back to the registers 200 at a single destination "dst2" and two different sources "src1" and "src2" are used for the inputs to the arithmetic logic unit 230.

Accordingly, clearly **the arithmetic operations are not performed on results of the multiply operations** in response to a single instruction. In contrast, claim 40 pertains to generating result data elements each including a **sum of intermediate data elements generated by multiplying** together corresponding initial data elements in a first packed data and a second packed in response to a single instruction.

Furthermore, claim 40 requires that the "intermediate data elements" resulting from the multiplications are divided into sets, and that the intermediate data elements within a "first" and "second" of the sets are separately summed. By way of example, and not limitation, as shown in Table 3b of the present patent application, two result data elements are each generated by summing two adjacent 32-bit intermediate results within a "packed data" format. In contrast, refer again to Table 21, and the A+B and A-B operations discussed above. According to these operations, the data input to the B-port is either added to, or subtracted from, the data input to the A-port, respectively.

For at least one or more of these reasons, claim 40 is believed to be allowable over Guttag. Claims 41-44 and 128 depend from claim 40 and are believed to be allowable therefor, as well as for the recitations set forth in each of these dependent claims.

Claim 1 recites: "*An apparatus for use in a computer system comprising: a memory having stored therein a first packed data comprising at least four data elements and a second packed data comprising at least four data elements; and a processor coupled to said memory to receive said first packed data and said second packed data, said processor performing operations on data elements in said first packed data and said second packed data to generate a plurality of data elements in a third packed data in response to receiving an instruction, at least two of said plurality of data elements in said third packed data storing the result of multiply-add operations*".

Guttag does not teach or suggest these limitations. In particular, describes a multiply and add (MPYx||ADD). The "||" represent parallel operation, and thus a separation and independence between the multiply operation and the add operation. This is not the claimed "multiply-add." In the claimed "multiply-add" there is a relationship between the output of the multiply operations and the add operation. Specifically, the

output of the multiply operations are the input to the add operation in a multiply-add operation (as indicated by the "-" symbol).

For at least one or more of these reasons, claim 1 is believed to be allowable over Guttag. Claims 27-31 depend from claim 1 and are believed to be allowable therefor, as well as for the recitations set forth in each of these dependent claims.

New Claims

New independent claim 133 recites an apparatus comprising "*a memory to store a first packed data including at least four data elements and a second packed data including at least four data elements; and a processor coupled with the memory to receive the first packed data and the second packed data, the processor to perform operations on data elements in the first packed data and the second packed data to generate a plurality of data elements in a third packed data in response to receiving an instruction, at least two of the plurality of data elements in the third packed data resulting from multiply-add operations*".

As discussed above for claim 1, Guttag does not teach or suggest these limitations. Accordingly, claim 133 is believed to be allowable over Guttag. Claims 134-135 depend from claim 133 and are believed to be allowable therefor, as well as for the recitations set forth in each of these dependent claims.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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